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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,834	12/27/2001	Brett W. Murdock	1280.SC11318TH	9616

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,834	MURDOCK ET AL.	
	Examiner	Art Unit	
	Midys Inoa	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7* is/are allowed.

6)☒ Claim(s) *1-6 and 8-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed February 14, 2005, with respect to the rejection(s)of claim(s) 1-6 and 8-21 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Chang (2003/0005247) in combination with Hahm (6,223,646).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 8-10, 16, 18-19, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang (2003/0005247 A1) in view of Hahm (6,223,646).

Regarding Claims 1, 10, 19, and 21, Chang teaches a memory access system (Figure 3) in which a first output (Figure 3, SMI signal) provides a first data lane enable to the SMM 180 and in a first normal mode of operation, the SMM utilizes the SMI signal for facilitating access of a portion of a first memory storage location associated with a first memory address within memory 140 (real mode 100); and when in a second mode of operation to access memory data with an address beyond 1 Mbyte, utilizing the SMI signal (first output) for facilitating designation of a second memory storage location (addressing range beyond 1Mbyte) within memory 140. Since the two memory modes of Chang denote different address thresholds to be accessed, the first and second modes facilitate access to different memory storage locations and thus provide different

address portions (See Figure 3, Claim 1, and paragraph 0033). The SMI signal facilitates access in this system by providing an interrupt when needed, since this signal comes from one source, the software interrupt interface 160, the system is utilizing the output of one port to perform at either mode of operation. Additionally, the mode of operations taken into account in the system of Chang, are the normal mode of accessing at the usual range and a second mode to access data with an address beyond 1 Mbyte.

Chang does not teach the first output being coupled directly to the memory. Hahm discloses a memory interface wherein a controlling module (FPGA 100) outputs an enable signal, an address signal, a data signal, a read signal, and a write signals and these outputs are directly coupled to a memory 300 (See Figure 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang so that its control structure (comprising real mode 100, software interrupt 160, and SMM 180) are all integrated into a single component performing all appropriate functions, as in the system of Hahm, since doing so allows for simplified connectivity. In integrating the components in the system of Chang, the outputs of such a system would be directly coupled to the memory 140.

Regarding Claim 16, Chang discloses a memory access system comprising Real Mode 100 having an output (software interrupt request) to indicate one of a first mode of operation and a second mode of operation; an address control portion 160 having an input coupled to the output of Real Mode 100, and an output (SMI Signal) which provides a first data lane enable to the SMM 180 and in a first normal mode of operation, the SMM utilizes the SMI signal for facilitating access of a portion of a first memory storage location associated with a first memory address within memory 140 (real mode of operation 100); and when in a second mode of

operation to access memory data with an address beyond 1 Mbyte, utilizing the SMI signal (first output) for facilitating designation of a second memory storage location (addressing range beyond 1Mbyte) within memory 140 (See Figure 3, Claim 1, and paragraph 0033). The SMI signal facilitates access in this system by providing an interrupt when needed, since this signal comes from one source, the software interrupt interface 160, the system is utilizing the output of one port to perform at either mode of operation. Additionally, the mode of operations taken into account in the system of Chang, are the normal mode of accessing at the usual range and a second mode to access data with an address beyond 1 Mbyte.

Chang does not teach the first output being coupled directly to the memory. Hahm discloses a memory interface wherein a controlling module (FPGA 100) outputs an enable signal, an address signal, a data signal, a read signal, and a write signals and these outputs are directly coupled to a memory 300 (See Figure 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang so that its control structure (comprising real mode 100, software interrupt 160, and SMM 180) are all integrated into a single component performing all appropriate functions, as in the system of Hahm, since doing so allows for simplified connectivity. In integrating the components in the system of Chang, the outputs of such a system would be directly coupled to the memory 140.

Regarding Claims 2-4, when accessing a memory it is possible to access memories of different widths. Since Chang teaches the accessing of "addressing ranges" which are being accessed independent in different accessing modes, it is understood that the system could be modified so that these addressing ranges could be represented by independent memories, which

could be byte wide or word wide. Additionally, since a word is always bigger than a byte (which is 8 bits) it is understood that a word wide memory has more than 8 bits associated with it. Regarding Claim 5, Chang discloses the first output being the first output of a first device 100; and the first and second modes of operation utilize the first output to access a second device 140 external to the first device.

Regarding Claims 8-9, 18, Chang teaches determining the mode of operation when the system realizes which address range needs to be accessed. If the system discovers that the first address range needs to be accessed, it determines that the first mode of operation needs to be in place. The same goes for the scenario when the second address range needs to be accessed. Additionally, the operation which requests the access to one address over another essentially performs as a chip select for the addressing range to be accessed ("a specific chip select", see Page 4, claim 1).

4. Claims 6, 11-15, and 20 are rejected under 35 USC 103 a as being unpatentable over Chang in view of Hahm and further in view of Microsoft Computer Dictionary, where the Microsoft Computer Dictionary is used as an evidentiary reference.

Regarding Claim 6, Chang in view of Hahm disclose the invention as set forth by claim 5 above. Chang in view of Hahm does not teach a third mode of operation in which the system accesses internal storage (a third addressing range). Since computer systems are known to have internal primary storage for their direct access (see Microsoft Computer Dictionary, Page 355), it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into Chang's system the use of a third mode of operation tracking internal primary

storage accesses (third addressing range), thus allowing the system to more accurately monitor accesses to all available storage.

Regarding Claims 11 and 14, Chang teaches a memory access system in which a first mode of operation is used to access a first addressing range (Real Mode 100) and a second mode of operation is used to access a second addressing range (access data with address beyond 1 Mbytes). Chang does not teach the set of output pins being coupled to a memory. Hahm discloses a memory interface wherein a controlling module (FPGA 100) outputs an enable signal, an address signal, a data signal, a read signal, and a write signals and these outputs are directly coupled to a memory 300 (See Figure 1). In Hahm individual output pins are represented by individual output lines. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang so that its control structure (comprising real mode 100, software interrupt 160, and SMM 180) are all integrated into a single component performing all appropriate functions, as in the system of Hahm, since doing so allows for simplified connectivity. In integrating the components in the system of Chang, the outputs of such a system would be directly coupled to the memory 140. Chang in view of Hahm does not teach accessing a third addressing range. Since computer systems are known to have internal primary storage for their direct access (see Microsoft Computer Dictionary, Page 355), it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into Chang's system the use of a third mode of operation tracking internal primary storage accesses (third addressing range), thus allowing the system to more accurately monitor accesses to all available storage. Since the unmodified system of Chang only has two mode of operation, only one lane enable is necessary for it operation. However, it is understood that in

adding another mode of operation more lane enables and chip selects are needed in order to differentiate between operation modes and addressing ranges.

Regarding Claims 12 and 13, when accessing a memory, it is possible for a system to access memories in locations remote and near, as long as access paths are present. Since Chang teaches the accessing of "addressing ranges" which are being accessed independent in different accessing modes, the system could be modified so that these addressing ranges could be represented by independent memories, which could be of the internal type within the main system, or of the external type outside of the main system.

Regarding Claim 15, Chang teaches a memory access system in which a first mode of operation is used to access a first addressing range (Real Mode 100) and a second mode of operation is used to access a second addressing range (access data with address beyond 1 Mbytes). Since the two memory modes of Chang denote different address thresholds to be accessed, the first and second modes facilitate access to different memory storage locations and thus provide different address portions (See figure 3, Claim 1, and paragraph 033). Chang does not teach the set of output pins being coupled to a memory. Hahm discloses a memory interface wherein a controlling module (FPGA 100) outputs an enable signal, an address signal, a data signal, a read signal, and a write signals and these outputs are directly coupled to a memory 300 (See Figure 1). In Hahm individual output pins are represented by individual output lines. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Chang so that its control structure (comprising real mode 100, software interrupt 160, and SMM 180) are all integrated into a single component performing all appropriate functions, as in the system of Hahm, since doing so allows for simplified

connectivity. In integrating the components in the system of Chang, the outputs of such a system would be directly coupled to the memory 140. Since computer systems are known to have internal primary storage for their direct access (see Microsoft Computer Dictionary, Page 355), it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into Chang's system the use of a third mode of operation tracking internal primary storage accesses (third addressing range), thus allowing the system to more accurately monitor accesses to all available storage. If three modes of operation are provided in the system, the three different addressing thresholds could be accessed through three different address bit locations (A(1), A(0), and A(n+1)).

Regarding Claim 20, Chang in view of Hahm teach the invention as set forth in Claim 19 above. Chang in view of Hahm does not teach the use of a third mode of operation to access a third memory device, which is internal to the system. Since computer systems are known to have internal primary storage for their direct access (see Microsoft Computer Dictionary, Page 355), it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate into Chang's system the use of a third mode of operation tracking internal primary storage accesses (third addressing range), thus allowing the system to more accurately monitor accesses to all available storage. Additionally, it is possible for a system to access memories in locations remote and near, as long as access paths are present. Since Chang teaches the accessing of "addressing ranges" which are being accessed independent in different accessing modes, it is understood that the system could be modified so that these addressing ranges could be represented by independent memories, which could be of the internal type within the main system, or of the external type outside of the main system.

5. Claim 17 is rejected under 103(a) as being unpatentable over Chang in view of Hahm and further in view of the Authoritative Dictionary of IEEE Standard Terms, where the IEEE Dictionary is being used as an evidentiary reference.

Regarding Claim 17, Chang in view of Hahm teaches the invention as set forth by claim 16 above. Chang in view of Hahm does not specifically teach a multiplexor used to select from two inputs and produce an output. In systems where a selection is being made from two modes of operations, it is common to use a multiplexor to enable the selection (see IEEE Dictionary, Page 716). It would have been obvious to one of ordinary skill in the art at the time the invention was made use a multiplexor in the system of Chang for selection purposes since a multiplexor enables for quick signal selections.

Allowable Subject Matter

6. Claim 7 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The Prior Art of Record does not teach an address bit used to extend an address range when a memory having a width less than a word is being accessed.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 27, 2005

Midys Inoa
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MI

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